WHAT IS CLAIMED IS:

1. A non-volatile semiconductor memory device comprising:

a plurality of columns each of which is connected with a plurality of memory cells;

a column selection circuit for selecting a part of the plurality of columns in response to a column address; and

a plurality of sense amplifier groups connected to columns selected by the column selection circuit,

wherein the column selection circuit is configured to select the columns determined by whether the column address is 4N-aligned (N being a positive integer of 1 or more).

2. The memory device according to claim 1, wherein the column selection circuit selects columns of the column address when the column address is 4N-aligned, and selects columns of a upper column address when the column address is not 4N-aligned.

3. The memory device according to claim 1, wherein the column selection circuit comprises:

a gate circuit for selecting a part of the columns in response to first column selection signals and second column selection signals;

a decoder for generating the first column selection signals in response to a first part of the column address; and

a judging circuit configured to determine whether the column address is 4N-aligned, based on a second part of the column address, wherein the judging circuit is structured to generate the second column selection signals so that the gate circuit selects either columns of the column address or columns of an upper column address.

4. The memory device according to claim 3, wherein the second column address comprises at least two least significant bits of the column address.

5. The memory device according to claim 3, wherein the columns are divided into a plurality of column groups each corresponding to the plurality of sense amplifier groups and the gate circuit comprises a plurality of column gate units each corresponding to the plurality of column groups.

6. The memory device according to claim 5, wherein each of the plurality of column gate units comprises:

a selecting circuit configured to select a first one of columns of a corresponding column group in response to the first and second column selection signals when the column address is 4N-aligned; and

a second selecting circuit configured to select a second one of the columns of the corresponding column group in response to the first and second column selection signals when the column address is not 4N-aligned,

wherein the first bit line corresponds to the column address and the second bit line corresponds to a upper one of the column address.

7. The memory device according to claim 5, wherein each of the plurality of column groups comprises first, second, third, and fourth columns, the first column selection signals comprises four column selection signals, and the second column selection signals comprises two column selection signals.

8. The memory device according to claim 7, wherein each of the plurality of column gate units comprises:

first and second transistors connected in series between the first column and a sense amplifier of a corresponding sense amplifier group; third and fourth transistors connected in series between the second column and the sense amplifier; fifth and sixth transistors connected in series between the third column and the sense amplifier; seventh and eighth transistors connected in series between the fourth column and the sense amplifier; ninth and tenth transistors connected in series between the second column and the sense amplifier; eleventh and twelfth transistors connected in series between the third column and the sense amplifier; and thirteenth and fourteenth transistors connected in series between the fourth column and the sense amplifier.

9. The memory device according to claim 8, wherein the first and ninth transistors are controlled by a first one of the first column selection signals, the third and eleventh transistors are controlled by a second one thereof, the fifth and thirteenth transistors are controlled by a third one thereof, the seventh transistor is controlled by a fourth one thereof, the second, fourth, sixth and eighth transistors are controlled by one of the second

column selection signals, and the tenth, twelfth and fourteenth transistors are controlled by the other one of the second column selection signals.

10. The memory device according to claim 9, wherein the one of the second column selection signals is activated when the column address is 4N-aligned.

11. The memory device according to claim 9, wherein the other one of the second column selection signals is activated when the column address is not 4N-aligned.

12. A non-volatile semiconductor memory device for performing a burst read operation of a predetermined burst length, comprising:

a plurality of sectors each of which includes a plurality of local bit lines;

a plurality of global bit lines;

a first column selection circuit for selecting one of the sectors and connecting a part of local bit lines of a selected sector to the plurality of global bit lines, respectively, based on a first part of a column address;

a plurality of sense amplifier groups each of which includes a plurality of sense amplifiers, the number of the sense amplifier groups corresponding to the burst length;

a second column selection circuit for selecting the plurality of global bit lines variably based on whether a second one of the column address for selecting the plurality of sense amplifier groups is 4N-aligned,

wherein, when the column address is not 4N-aligned, the second column selection circuit connects a sense amplifier group of the second column address and a upper sense amplifier group(s) to global bit lines of the column address, and connects remaining lower sense amplifier groups to global bit lines of a upper column address.

13. The memory device according to claim 12, wherein, when the column address is 4N-aligned, the second column selection circuit connects the plurality of sense amplifier groups to global bit lines of the column address.

14. The memory device according to claim 12, wherein the second column address comprises at least two least significant bits of the column address.

15. The memory device according to claim 12, wherein the first column selection circuit comprises:

a first decoder for generating column selection signals in response to a part of the first column address;

a plurality of first column gate units each corresponding to the sectors and each selecting a part of local bit lines of a corresponding sector in response to the column selection signals;

a second decoder for generating sector selection signals in response to another part of the first column address; and

a plurality of sector selectors each corresponding to the sectors and each connecting the global bit lines to local bit lines selected by a corresponding first column gate unit, respectively.

16. The memory device according to claim 12, wherein the second column selection circuit comprises:

a column gate circuit for selecting a part of the global bit lines in response to first column selection signals and second column selection signals;

a decoder for generating the first column selection signals in response to a first part of the second column address; and

a judging circuit for determining whether the column address is 4N-aligned, based on a second part of the second column address, wherein the judging circuit generates the second column selection signals so that the second column gate circuit selects either global bit lines of the column address or global bit lines of a upper column address.

17. The memory device according to claim 16, wherein the global bit lines are divided into a plurality of groups each corresponding to the plurality of sense amplifier groups and the second column gate circuit comprises a plurality of column gate units corresponding to the plurality of groups of global bit lines.

18. The memory device according to claim 17, wherein each of the plurality of column gate units comprises:

a selecting circuit for selecting a first one of global bit lines of a corresponding group in response to the first and second column selection signals when the column address is 4N-aligned; and

a second selecting circuit for selecting a second one of the global bit lines of the corresponding group in response to the first and second column selection signals when the column address is not 4N-aligned.

19. The memory device according to claim 18, wherein each of the plurality of groups of global bit lines comprises first, second, third, and fourth global bit lines, the first column selection signals comprises four column selection signals, and the second column selection signals comprises two column selection signals.

20. The memory device according to claim 19, wherein the selecting circuit comprises:

first and second transistors connected in series between the first global bit line and a sense amplifier of a corresponding sense amplifier group; third and fourth transistors connected in series between the second global bit line and the sense amplifier; fifth and sixth transistors connected in series between the third global bit line and the sense amplifier; and seventh and eighth transistors connected in series between the fourth global bit line and the sense amplifier,

the first, third, fifth and seventh transistors being controlled by the first column selection signals respectively; and the second, fourth, sixth and eighth transistors being controlled by one of the second column selection signals.

21. The memory device according to claim 20, wherein the one of the second column selection signals is activated when the column address is 4N-aligned.

22. The memory device according to claim 20, wherein the second selecting circuit comprises:

ninth and tenth transistors connected in series between the second global bit line and the sense amplifier; eleventh and twelfth transistors connected in series between the third global bit line and the sense amplifier; and thirteenth and fourteenth transistors connected in series between the fourth global bit line and the sense amplifier,

the ninth, eleventh and thirteenth transistors being controlled by first, second, and third ones of the first column selection signals, respectively; and the tenth, twelfth and fourteenth transistors being controlled by the other of the column selection signals.

23. The memory device according to claim 22, wherein the other of the second column selection signals is activated when the column address is not 4N-aligned.

24. A NOR-type flash memory device comprising:

a plurality of bit lines each of which is connected with a plurality of non-volatile memory cells;

a column gate circuit for selecting at least one of the bit lines in response to first selection signals and second selection signals;

at least one sense amplifier connected to a bit line selected by the column gate circuit;

a decoder circuit for generating the first selection signals in response to a first part of a column address; and

means for judging whether the column address is 4N-aligned, based on a second part of the column address, and generating the second selection signals,

wherein the column gate circuit comprises a first switch circuit for selecting a first one of the bit lines in response to the first and second selection signals when the column address is 4N-aligned; and a second switch circuit for selecting a second one of the bit lines in response to the first and second selection signals when the column address is not 4N-aligned.

25. The memory device according to claim 24, wherein the bit lines comprises first, second, third, and fourth bit lines, the first selection signals comprises four column selection signals, and the second selection signals comprises two column selection signals.

26. The memory device according to claim 25, wherein the first switch circuit comprises:

first and second transistors connected in series between the first bit line and the sense amplifier; third and fourth transistors connected in series between the second bit line and the sense amplifier; fifth and sixth transistors connected in series between the third bit line and the sense amplifier; and seventh and eighth transistors connected in series between the fourth bit line and the sense amplifier,

the first, third, fifth and seventh transistors being controlled by the first selection signals respectively; and the second, fourth, sixth and eighth transistors being controlled by one of the second selection signals.

27. The memory device according to claim 26, wherein the one of the second column selection signals is activated when the column address is 4N-aligned.

28. The memory device according to claim 26, wherein the second switch circuit comprises:

ninth and tenth transistors connected in series between the second bit line and the sense amplifier; eleventh and twelfth transistors connected in series between the third bit line and the sense amplifier; and thirteenth and fourteenth transistors connected in series between the fourth bit line and the sense amplifier,

the ninth, eleventh and thirteenth transistors being controlled by first, second and third ones of the first selection signals respectively; and the tenth, twelfth and fourteenth transistors being controlled by the other of the second selection signals.

29. The memory device according to claim 28, wherein the other of the second column selection signals is activated when the column address is not 4N-aligned.

30. The memory device according to claim 24, wherein a bit line selected by the first switch circuit corresponds to the column address and a bit line selected by the second switch circuit corresponds to a upper one of the column address.

31. A NOR-type flash memory device comprising:

first, second, third, and fourth bit lines;

at least one sense amplifier; and

a column gate circuit for connecting one of the bit lines to the at least one sense amplifier,

wherein the column gate circuit comprises:

first and second transistors connected in series between the first bit line and the sense amplifier and controlled by first and second control signals, respectively;

third and fourth transistors connected in series between the second bit line and the sense amplifier and controlled by a third control signal and the second control signal, respectively;

fifth and sixth transistors connected in series between the third bit line and the sense amplifier and controlled by a fourth control signal and the second control signal, respectively;

seventh and eighth transistors connected in series between the fourth bit line and the sense amplifier and controlled by a fifth control signal and the second control signal, respectively;

ninth and tenth transistors connected in series between the second bit line and the sense amplifier and controlled by the first control signal and a sixth control signal, respectively;

eleventh and twelfth transistors connected in series between the third bit line and the sense amplifier and controlled by the third and sixth control signals, respectively; and

thirteenth and fourteenth transistors connected in series between the fourth bit line and the sense amplifier and controlled by the fourth and sixth control signals, respectively.

32. The memory device according to claim 31, wherein the second control signal is activated when a column address for selecting the bit lines is 4N-aligned and the sixth control signal is activated when the column address is not 4N-aligned.

33. A flash memory device comprising:

a sector having memory cells connected with a plurality of bit lines;

a plurality of gate circuits connected to the plurality of bit lines and receiving first column select signals and second column select signals; and

a plurality of sense amplifier groups each connected to the gate circuits and having a plurality of unit sense amplifiers,

wherein the gate circuits are configured such that the first column select signals are controlled in common and the second column select signals are controlled individually.

34. The flash memory device according to claim 33, wherein each of the gate circuits includes a plurality of gate units.

35. The flash memory device according to claim 34, wherein each of the gate units includes a first switch for receiving the first column select signals and a second switch for receiving the second column select signals, the first and second switches being cascaded to each other.

36. The flash memory device according to claim 34, wherein each of the gate units includes a first current path and a second current path formed between a corresponding bit line and a corresponding unit sense amplifier, the first and second current path being connected in parallel.

37. The flash memory device according to claim 34, wherein each of the gate units includes at least one parallel current path placed between a corresponding bit line and a corresponding unit sense amplifier.

38. The flash memory device according to claim 33, further comprising:

a decoder for decoding a column address to generate the first column select signals; and

a judging circuit for determining whether the column address is 4N-aligned to generate the second column select signals.

39. The flash memory device according to claim 36, wherein each of the first and second current paths includes first and second NMOS transistors, the first NMOS transistor being controlled by a corresponding first column select signal and the second NMOS transistor being controlled by a corresponding second column select signal.